PRELIMINARY

SOLID STATE DEVICES, INC

14849 Firestone Boulevard · La Mirada,CA 90638
Phone: (714) 670-SSDI (7734) · Fax: (714) 522-7424

SFF40N10-28

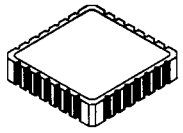
Designer's Data Sheet

40* AMP
100 VOLTS
0.055Ω
N-CHANNEL
POWER MOSFET

FEATURES:

- Rugged construction with poly silicon gate
- Low RDS(on) and high transconductance
- Excellent high temperature stability
- Very fast switching speed
- Fast recovery and superior dv/dt performance
- Increased reverse energy capability
- Low input and transfer capacitance for easy paralleling
- Hermetically sealed surface mount package
- TX, TXV and Space Level screening available
- Replaces: SMP40N10 Types

28 PIN CLCC



MAXIMUM RATINGS

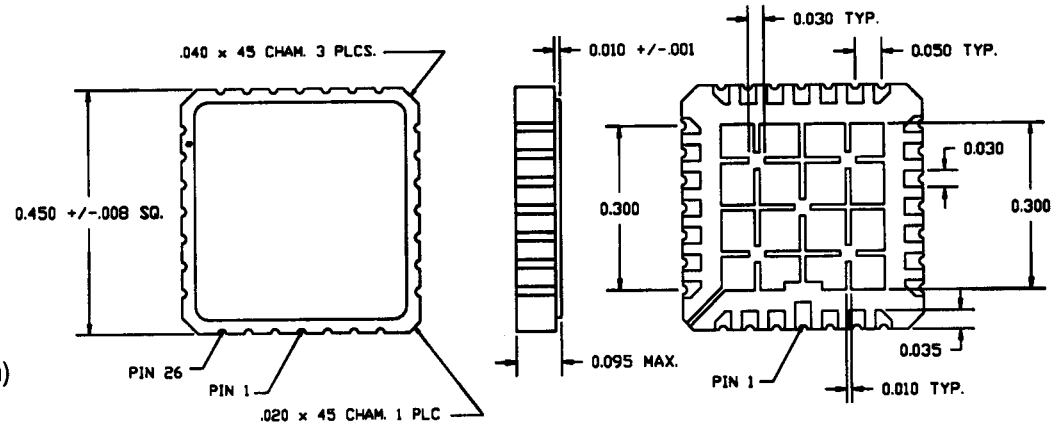
CHARACTERISTIC	SYMBOL	VALUE	UNIT
Drain to Source Voltage	V_{DS}	100	Volts
Gate to Source Voltage	V_{GS}	±20	Volts
Continuous Drain Current	I_D	40*	Amps
Operating and Storage Temperature	T_{op} & T_{stg}	-55 to +150	°C
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Total Device Dissipation @ TC=25°C Total Device Dissipation @ TA=95°C	P_D	50* 30	Watts

PACKAGE OUTLINE: 28 PIN CLCC

PIN OUT:
SOURCE: 1, 15- 28
DRAIN: 5-11
GATE: 2, 3, 13, 14

NOTE:

All Drain/Source Pins must be connected on the PC Board in order to maximize current capability and minimize RDS(on)



*** Rating based on size of chip. Device rating may vary depending on mounting and heatsink conditions. Consult SSDI Marketing department for thermal derating details.**

NOTE: All specifications are subject to change without notification. SCD's for these devices should be reviewed by SSDI prior to release.	**DATA SHEET #: F00001 A**	**MED**

SFF40N10-28

PRELIMINARY

SOLID STATE DEVICES, INC

14849 Firestone Boulevard · La Mirada,CA 90638
Phone: (714) 670-SSDI (7734) · Fax: (714) 522-7424

ELECTRICAL CHARACTERISTICS @ TJ=25 C (Unless Otherwise Specified)

RATING		SYMBOL	MIN	TYP	MAX	UNIT
Drain to Source Breakdown Voltage (VGS=0 V, ID=250μA)		BV_{DSS}	100	---	---	V
Drain to Source on State Resistance (VGS=10 V, ID= 25 A)		$R_{DS(on)}$	---	0.045	0.055**	Ω
On State Drain Current (VDS=5V, VGS=10 V)		$I_{D(on)}$	40*	---	---	A
Gate Threshold Voltage (VDS=VGS, ID=250μA)		$V_{GS(th)}$	2.0	---	4.0	V
Forward Transconductance (VDS=15V, IDS=60% rated ID)		g_{fs}	10	25	---	S(℧)
Zero Gate Voltage Drain Current (VDS=80V, VGS=0 V) (VDS=80% rated VDS, VGS=0 V, TJ=125°C)		I_{DSS}	--- ---	--- ---	25 250	μA
Gate to Source Leakage Forward Gate to Source Leakage Reverse	At rated VGS	I_{GSS}	--- ---	--- ---	100 -100	nA
Total Gate Charge Gate to Source Charge Gate to Drain Charge	VGS=10 Volts 80% rated VDS Rated ID	Q_g Q_{gs} Q_{gd}	--- --- ---	60 75 30	120 100 50	nC
Turn on Delay Time Rise Time Turn Off Delay Time Fall Time	Tj=100°C VDD=25V VGEN=10V ID=20A RG=50Ω	$t_{d(on)}$ t_r $t_{d(off)}$ t_f	--- --- --- ---	17 80 40 20	50 300 150 100	nsec
Diode Forward Voltage (IS=rated ID, VGS=0 V, TJ=25°C)		V_{SD}	---	1	2	V
Diode Reverse Recovery Time Reverse Recovery Charge	TJ=25°C IF=rated ID di/dt=100 A/ sec	t_{rr} Q_{RR}	--- ---	120 0.3	250 ---	nsec μC
Input Capacitance Output Capacitance Reverse Transfer Capacitance	VGS=0 Volts VDS=25 Volts f= 1 MHz	Ciss Coss Crss	--- --- ---	3000 750 150	5000 2500 1000	pF

For thermal derating curves and other characteristic curves please contact SSDI Marketing Department.

NOTES:

* Rating based on size of chip. Device rating may vary depending on mounting and heatsink conditions. Consult SSDI Marketing department for thermal derating details.

** Due to package resistance; all Source/Drain pins must be connected on the PC Board in order to obtain the lowest RDS(on) possible.